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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
10/687,271	10/16/2003	Olubunmi O. Adetutu	SC12752TP 9985		
23125	7590 01/24/2006		EXAMINER		
FREESCALE SEMICONDUCTOR, INC.			SCHILLINGER, LAURA M		
LAW DEPARTMENT 7700 WEST PARMER LANE MD:TX32/PL02			ART UNIT	PAPER NUMBER	
	AUSTIN, TX 78729			2813	
			DATE MAILED: 01/24/2006		

Please find below and/or attached an Office communication concerning this application or proceeding.

•	Application No.	Applicant(s)			
· — ·	10/687,271	ADETUTU ET AL			
Office Action Summary	Examiner	Art Unit			
	Laura M. Schillinger	2813			
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply					
A SHORTENED STATUTORY PERIOD FOR REPLY WHICHEVER IS LONGER, FROM THE MAILING DATE - Extensions of time may be available under the provisions of 37 CFR 1.13 after SIX (6) MONTHS from the mailing date of this communication. If NO period for reply is specified above, the maximum statutory period we failure to reply within the set or extended period for reply will, by statute, Any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b).	ATE OF THIS COMMUNICATION 36(a). In no event, however, may a reply be tim vill apply and will expire SIX (6) MONTHS from cause the application to become ABANDONEI	N. nely filed the mailing date of this communication. D (35 U.S.C. § 133).			
Status					
 1) ☐ Responsive to communication(s) filed on 11 Octobre 2a) ☐ This action is FINAL. 2b) ☐ This 3) ☐ Since this application is in condition for alloware closed in accordance with the practice under Expression in the practice of the practice of	action is non-final. nce except for formal matters, pro				
Disposition of Claims					
4) ☐ Claim(s) 1-42 is/are pending in the application. 4a) Of the above claim(s) 20-42 is/are withdraw 5) ☐ Claim(s) is/are allowed. 6) ☐ Claim(s) 1-9,11 and 13-19 is/are rejected. 7) ☐ Claim(s) 10 and 12 is/are objected to. 8) ☐ Claim(s) are subject to restriction and/or	n from consideration.				
Application Papers					
9) The specification is objected to by the Examine 10) The drawing(s) filed on is/are: a) access Applicant may not request that any objection to the Replacement drawing sheet(s) including the correction of the output of of the	epted or b) objected to by the Eddrawing(s) be held in abeyance. See ion is required if the drawing(s) is obj	e 37 CFR 1.85(a). lected to. See 37 CFR 1.121(d).			
Priority under 35 U.S.C. § 119					
12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of: 1. Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No. 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received.					
Attachment(s) 1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 10/6/05; 10/16/03.	4) lnterview Summary Paper No(s)/Mail Da 5) Notice of Informal P 6) Other:				

DETAILED ACTION

Election/Restrictions

Applicant's election of claims 1-19 in the reply filed on 6/21/05 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-9, 11, 13-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Shimamoto et al ('451).

1. A method for forming a dielectric comprising:

forming a first dielectric layer (2) over semiconductor material (1) (Fig. 1);

introducing a diffusion barrier material into the first dielectric layer (3); and

forming a second dielectric layer (4 or nitrided SiO) over the first dielectric layer after the introducing (Col.12, lines:30-Col.14, line:55- all describing Fig.1).

- 2. The method of claim 1 wherein the diffusion layer material includes nitrogen (Col.15, lines: 45-65).
- 3. The method of claim 1 wherein the second dielectric layer is a relatively higher K dielectric than the first dielectric layer (Col.4, lines: 20-25).
- 4. The method of claim 1 wherein the introducing further includes: performing plasma processing of the diffusion barrier material into the first dielectric layer (Col.15-16, lines: 45-25).
- 5. The method of claim 1 wherein the introducing further includes: implanting the diffusion barrier material into the first dielectric layer (Col.15-16, lines: 45-25).
- 6. The method of claim 1 wherein the introducing further includes: performing a thermal anneal of material including the diffusion barrier material into the first dielectric layer (Col. 15-16, lines: 45-25).
- 7. The method of claim 1 wherein the semiconductor material includes silicon (Col. 12, lines: 30-35).

- 8. The method of claim 7 wherein the semiconductor material includes at least one of single crystal silicon, strained silicon, or silicon germanium(Col. 12, lines: 30-35).
- 9. The method of claim 1 wherein the first dielectric layer includes silicon oxide (Col.15-16, lines: 45-25).

- 11. The method of claim 1 wherein the second dielectric layer includes silicon nitride ((Col.15-16, lines: 45-25).
- 13. The method of claim 1 wherein the second dielectric layer includes a high K dielectric (Col.4, lines: 20-25).
- 14. The method of claim 1 wherein the high K dielectric includes at least one of a metal oxide, a metal silicate, a metal oxynitride, and a metal silicon oxynitride (Col.4, lines: 20-25).

- 15. The method of claim 14 wherein: the metal oxide includes at least one of hafnium oxide, aluminum oxide, lanthanum oxide, titanium oxide, and tantalum oxide; the metal silicate includes at least one of hafnium silicate, aluminum silicate, lanthanum silicate, titanium silicate, and tantalum silicate', the metal oxynitride includes at least one of hafnium oxynitride, aluminum oxynitride, lanthanum oxynitride, titanium oxynitride, and tantalum oxynitride; and the metal silicon oxynitride includes at least one of hafnium silicon oxynitride, aluminum silicon oxynitride, lanthanum silicon oxynitride, titanium silicon oxynitride, and tantalum silicon oxynitride (Col.4, lines: 20-25).
- 16. The method of claim 1 wherein after the introducing, the diffusion material has a gradual gradient profile in the first dielectric layer (Col.15-16, lines: 45-25-inherent characteristic of the nitriding process).
- 17. The method of claim 1 wherein after the introducing, a bottom portion of the first dielectric layer has lower concentration of the diffusion barrier material than an upper portion of the first dielectric layer (Col. 15-16, lines: 45-25).
- 18. The method of claim 1 wherein the introducing forms a barrier layer including the diffusion barrier material in an upper portion of the first dielectric layer (Col. 15-16, lines: 45-25)..
- 19. The method of claim 1 further comprising:

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forming a layer of gate material over the second dielectric layer;

patterning the layer of gate material to form a gate from the layer of gate material, the gate located over the second dielectric layer (Fig. 1 (5)).

Allowable Subject Matter

The following is a statement of reasons for the indication of allowable subject matter:

Prior art of record fails to teach nor suggest the limitations of claims 10 and 12.

Claims 10 and 12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Laura M. Schillinger whose telephone number is (571) 272-1697. The examiner can normally be reached on M-T, R-F 7:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

01/22/06

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